REMARKS

Claim 5 has been amended to correct an original drafting error so that the process is a correctly integrated process. Support for the amendment of Claim 5 is found in the application Specification as originally filed at Page 18, line 33, continuing at Page 19, lines 1 and 2.

Claim 18 is objected to under 37 CFR § 1.75 as being a substantial duplicate of Claim 9. The Examiner states that "It appears that claim 18 may have been meant to depend on claim 14, instead of claim 1." The Examiner is correct in that Claim 18 was meant to depend on Claim 14, not Claim 1. In applicants' originally filed claim set, Claim 18 depended from Claim 14. Applicants' Preliminary Amendment "A", which was filed with the subject application, contained a typographical error in the claim set which indicated that Claim 18 depended from Claim 1, not Claim 14. Applicants have corrected the typographical error in the claim set presented above. Applicants do not believe that there is any need to formally amend Claim 18 to depend from Claim 14, because Claim 18 had not previously been formally amended to depend from Claim 1 (rather than its original dependency on Claim 14).

Claim Rejections Under 35 USC § 102

Claims 1, 10, 11, 13 - 16, 22, 23, 26, and 27 are rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 6,143,476, to Ye et al.

Applicants respectfully contend that their invention as claimed in Claims 1, 10, 11, 13 - 16, 22, 23, 26, and 27 is not anticipated by U.S. patent No. 6,143, 476 to Ye et al. Applicants contend that to have anticipation, every step in applicants' integrated process must be present in the Ye et al. process, and the Ye et al. process may not require additional steps over those specified by applicants to accomplish the same result. However, the Ye et al. invention pertains to a method of patterning a semiconductor device feature which provides for the easy removal of residual hard masking layer which remains after completion of a pattern etching process (Col. 2, lines 42 - 60). To obtain easy removal of the hardmasking layer, an organic layer is applied between the hardmasking layer and

the underlying substrate which is to be pattern etched. Applicants' method does not make use of an organic layer between the hard masking layer, which is specified to be an inorganic masking layer, and the underlying substrate which is to be pattern etched. Therefore, applicants' invention is not anticipated by the disclosure in the Ye et al. patent. In fact, the Ye et al. patent teaches away from applicants' invention.

In more detail, the concept in the Ye et al. reference is that the hard masking layer is typically a good dielectric and that presence of the residual hard masking layer decreases the gate speed of a field effects transistor, for example. Thus, it is necessary to be certain that the residual hard masking layer can be easily removed. (Col. 2, lines 61 - 65) The Ye et al. method provides for a multi-layered masking structure which includes a layer of high temperature, organic-based masking material, overlaid by either: 1) a layer of a high-temperature, inorganic masking material, which can be patterned to provide an inorganic hard mask, or 2) a layer of a high temperature, imageable, organic masking material, which can be patterned to provide an organic hard mask. The hard masking material is used to transfer a pattern to the high temperature, organic-based masking material, and may be used to transfer the pattern through a portion of an underling metal layer. In any case, the hard masking material is designed to be removed prior to completion of the metal layer etching, leaving only high temperature organic-based masking material residue after completion of the metal etch, since this residual material is easier to remove from the metal surface. (Col. 9, lines 41 - 47 and Col. 10, lines 4 - 13).

The Ye et al. reference teaches away from the present invention in teaching that it is a disadvantage to have an inorganic material applied directly over a conductive material during patterning of the conductive material, as the inorganic hard masking layer is difficult to remove subsequently. (Col. 2, lines 42 - 67.) In applicants' method, the layer directly overlying (on) the conductive noble metal layer to be etched is an inorganic protective layer (independent Claims 1 and 14) or an inorganic hard masking layer (Claims 13, 19, and 22).

The Ye et al. reference neither teaches or even suggests the specific combinations of materials and integrated processes which are taught by applicants. In light of the above distinctions, applicants respectfully request withdrawal of the rejection of Claims 1, 10, 11, 13 - 16, 22, 23, 26, and 27 under 35 USC § 102(e), over Ye et al.

Claim Rejections Under 35 USC § 103

Claims 12 and 17 are rejected under 35 USC § 103(a) as being unpatentable over Ye et al. Claims 12 (which depends from Claim 1) and 17 (which depends from Claim 14), both pertain to the thickness of the inorganic mask layer which is applied over the inorganic protective layer which is applied over the conductive noble metal layer.

Applicants respectfully submit that Claims 12 and 17, which depend from Claims 1 and 14 are not obvious in view of the Ye et al. disclosure which teaches away from applicants' invention as claimed in Claims 1 and 14, as described above, regardless of the thickness of the inorganic masking layer.

In light of the above, applicants respectfully request withdrawal of the rejection of Claims 12 and 17 under 35 USC § 103(a), over Ye et al.

Claims 2 - 5 are rejected under 35 USC § 103(a) as being unpatentable over Ye et al., as applied to Claim 1, and further in view of U.S. Patent No. 6,046,113, to Hong et al.

Applicants respectfully contend that Claims 2 - 5 are not obvious over the combination of the Ye et al. and Hong et al. references. The Ye et al. reference teaches the requirement of an organic layer between an inorganic masking layer and an underlying substrate to be etched, while applicants apply their inorganic masking layer directly over the underlying substrate to be etched. The Hong et al. reference teaches the use of a combination of wet and dry etchants and applicants do not teach or claim the use of wet etchants. A combination of these two references, both of which

teach away from applicants' invention does not render applicants' invention as Claimed in Claims 2 - 5 obvious.

In more detail, applicants' Claims 2 - 4 depend from Claim 1, and pertain to the removal of residual noble metal layer, or residual protective layer material prior to a subsequent etch step. Amended Claim 5 depends from Claim 1 and recites that the protective layer is removed during pattern etching of the barrier layer. In any case, these claims are patentable over the Ye et al. reference for the reasons provided with respect to the patentability of Claim 1. Further, a combination of the steps recited in the dependent claims with the steps recited in Claim 1 is distinctly patentable as an integrated process which is not described or even suggested in the Ye et al. reference.

The Hong et al. reference pertains to a method of etching layers during fabrication of a semiconductor device which method employs a combination of dry and wet etch steps. (Col. 1, lines 45 - 50) Hong et al. is cited by the Examiner as teaching that residual layers remaining on a surface would interfere with later semiconductor processing. The need to remove residual layers during processing of a device structure has been recognized in the art. For example, the Ye et al. reference teaches that the presence of a residual layer such as a photoresist is likely to interfere during subsequent pattern transfer steps which are conducted at temperatures which tend to melt or distort the photoresist. (Col. 4, lines 31 - 36). However, the removal of layers which are not needed in the final device structure may occur during a series of integrated process steps only at a time such that the removal can be integrated into the process as a whole without harming the device structure which is to be obtained. Thus, it is the order in which a particular series of process steps is carried out which dictates when it is possible to remove undesired etch stack layers. The timing of the removal is unique to the structure being etched and to the manner in which etching is carried out. For example, applicants' etching is carried out using dry plasma etching while the etching described in the Hong et al. reference is carrier out using a combination of wet etching and dry etching. Applicants' method is one for patterning electrodes of RAM capacitors, while the Hong et al. method

is one for fabricating a transistor. (Col. 2, lines 21 - 24) A comparison of applicants' Figure 5 with the Hong et al. Figure 1A shows the difference in structure and materials which are present in the starting semiconductor etch stack. A comparison of applicants' Figure 16 with the Hong et al. Figure 1H shows the difference in structure and materials which are present in the finished device. It is readily apparent to one skilled in the art that the process steps required to get from applicants' starting structure to the final structure are totally different from those required in the Hong et al. reference.

The Examiner states that "It would have been obvious to one of ordinary skill in the art to remove the residual noble metal and residual protective layer in the method of Ye because Hong teaches that residual layers will interfere with later semiconductor processing". However, it is highly unlikely that one skilled in the art would combine the teachings in the Ye et al. reference with the teachings in the Hong et al. reference, due to the difference in device structure and etch methods described in these two references. Further, even if the teachings of these two references are combined, they do not lead in the direction of applicants' invention.

In light of the above distinctions, applicants respectfully request withdrawal of the rejection of Claims 2 - 5 under 35 USC § 103(a), over Ye et al., and further in view of Hong et al.

Claim 19 is rejected under 35 USC § 103(a) as being unpatentable over Ye et al., in view of U.S. Patent No. 4,456,675, to Anderson, Jr. et al. and U.S. Patent No. 5,948,570, to Kornblit et al.

Applicants respectfully contend that Claim 19 of applicants' invention is not obvious in view of a combination of the Ye et al., Anderson Jr. et al. and Kornblit et al. references. Claim 19 is an independent claim which recites that the inorganic mask layer directly overlies the noble metal layer, and thus this claim is not obvious over the teachings of Ye et al. The Anderson Jr. et al. process pertains to a "lift off" process where portions of a metal layer are removed by depolymerization of an underlying polymeric layer in the areas where the metal layer is to be removed. Applicants are using a dry etch process to pattern their noble metal and no lift off process is even suggested. A

combination of the Anderson Jr. et al. and the Ye et al. references will not lead to applicants' invention. The Kornblit et al. reference teaches a method of etching a chromium comprising layer using reactive ion etching where the plasma is generated from a gaseous mixture of oxygen, chlorine and nitrogen, where the patterned resist material is an organometallic material such as a polymer which contains silicon or germanium. Applicants plasma source gas as claimed in Claim 19 contains an additive selected from HBr, BCl_3 or mixtures thereof, none of which are even suggested in the Kornblit et al. reference. The addition of the teachings of the Kornblit et al. reference with those of Ye et al. and Anderson Jr. et al. does not motivate one skilled in the art to arrive at applicants' invention.

In detail, Claim 19 is an independent claim which recites a structure in which the inorganic mask layer in on (directly overlying) the noble metal layer, as illustrated and described with respect to Figure 1. There is no organic layer of the kind described and claimed in the Ye et al. reference present between the noble metal and the inorganic (hard) mask layer.

Anderson, Jr. et al. pertains to a process for forming a desired metal pattern on a substrate. The method comprises forming a mask of a thermally depolymerizable polymer on the substrate with a pattern of openings complementary to the desired metal pattern; blanket coating the substrate and the mask with a metal; heating the substrate to depolymerize the depolymerizable polymer; cooling the surface of the metal to delaminate the metal coated in areas where thermally depolymerizable polymer is present; removing the delaminated metal where necessary; and, optionally, plasma ashing the depolymerized polymer to remove residual depolymerized polymer from the substrate. (Abstract) This kind of process is often referred to as a "lift-off" process, since the metal is removed by delamination (and lift off) when the thermally depolymerizable polymer underlying the metal to be lifted off is depolymerized. There is no lift-off process involved in either applicants' method or in the Ye et al. method. The lift-off process was used back in 1984, before the dimensional requirements for the device structures became as small as they are today. The lift-off process often leaves behind loose pieces of metal which are large enough to totally disrupt the function of a

structure of the kind fabricated in the semiconductor industry today. It is unlikely that one skilled in the art would combine the teachings of the Anderson, Jr. et al. reference with those of the Ye et al. reference which uses organic polymers in a different manner, but even if these teachings are combined, the combination of teachings does not lead in the direction of applicants' invention as described and claimed.

Anderson, Jr. et al. is cited by the Examiner as teaching that silicon dioxide is a conventional etch stop material. Those skilled in the art would generally recognize that any material can be used as an etch stop material depending on the combination of gases which are used in the etch process. It is not helpful to take an individual teaching of the use of a material from a first process which is very disparate as a whole from a second process and to argue that it is obvious that the material would be substituted into the second process. Silicon dioxide can be used for a number of different purposes. Most often, silicon dioxide is used as a dielectric (electrically insulative) material in device structures. This is totally independent of whether it may be used as an etch stop layer. For example, if the etchant being used includes fluorine, a silicon dioxide layer may be etched away in short order.

Kornblit et al. pertains to a process for dry lithographic etching. Patterning of a layer of material such as chromium or a chromium-comprising layer is carried out by reactive ion etching from a gaseous mixture of oxygen, chlorine, and nitrogen. The mask for etching is a patterned organometallic resist, such as a polymer which contains silicon or germanium. (Abstract) Kornblit et al. is cited by the Examiner as teaching that a noble gas may be added to etchant gas mixtures in order to increase ion flux, stabilize the plasma, or both. Applicants would agree that it is generally known in the art that noble gases which are generally inert may be used as diluents within a plasma source gas. At the same time it is important tho note that the Kornblit et al. plasma source gas contains oxygen and nitrogen which are not present in applicants' plasma source gas and that applicants' plasma source gas contains an additive selected from HBr, BCl3, and mixtures thereof, none of which are present in the Kornblit et al. process. A combination of the Ye et al. method

(which interposes an organic material layer between the hardmasking layer and underlying substrate to be etched) with the Anderson Jr. et al. process (which employs a metal lift off technique not used by applicants) with the Kornblit et al. process (which employs a different combination of etchant gases from those used by applicants) will not lead one skilled in the art to applicants' invention as claimed in Claim 19.

In light of the above distinctions, applicants respectfully request withdrawal of the rejection of Claim 19 under 35 USC § 103(a), over Ye et al., in view of Anderson, Jr. et al. and Kornblit et al.

Claims 6, 9, 18, and 25 are rejected under 35 USC § 103(a) as being unpatentable over Ye et al., as applied to Claim 1 or 22, and further in view of U.S. Patent No. 5,591,671, to Kim et al.

Applicants respectfully contend that Claims 6, 9, 18, and 25 are not obvious over a combination of the Ye et al. and Kim et al. references. Claim 6 depends from Claim 1 and recites that the mask layer is formed from CVD SiO_2. Claims 9, 18, and 25 all pertain to various materials which may be used to form the masking layer, where there are 6 different materials listed and only one of these is silicon oxide. Claims 9 and 18 depend indirectly from Claim 1, and Claim 25 depends from Claim 22, which recites that a second mask layer resides upon a first mask layer, which resides on a noble metal layer, where both mask layers are formed from an inorganic material. Clearly claims 6, 9, 18, and 25 are distinct from the Ye et al. reference which teaches against the direct application of an inorganic masking layer over a substrate metal which is to be etched. The Kim et al. reference pertains to a method of producing multilayer metal connections using a dual damascene process. There is no description of the dry etching of electrodes of a RAM capacitor structure of the kind described by applicants. As a result, the method of fabricating the Kim et al. structure and the steps used in the method are considerably different from the steps described and claimed by applicants. A combination of the Kim et al. reference with the Ye et al. reference does not lead in the direction of applicants' invention.

In detail, the distinctions between the disclosure of Ye et al. and applicants' invention is discussed in detail above. Kim et al. pertains to a method for interconnecting layers in a semiconductor device which can form a low resistance contact. An insulating layer is formed on a semiconductor substrate, and an opening is formed in the insulating layer. The opening is a contact hole for exposing an impurity diffusion region formed on the semiconductor substrate, or a via hole for exposing a lower conductive layer formed on the semiconductor substrate. Subsequently, a titanium ohmic contacting layer and a titanium nitride barrier layer are formed on the semiconductor substrate. Thereafter, a refractory metal layer which completely fills the remainder of the opening hole is formed by depositing the refractory metal on the barrier layer. The resultant structure is heat-treated at a temperature above 450°C. As a result, oxidation of the ohmic contacting layer and the barrier layer is said to be prevented, and silicide is actively formed on the interface between the ohmic contacting layer and the silicon substrate. (Abstract)

Kim et al. is cited by the Examiner as teaching that CVD is a conventional method for depositing silicon oxide. The Examiner states "It would have been obvious to one of ordinary skill in the art in the method of Ye, Ye in view of Hong or Ye in view of Anderson and Kornblit to deposit the (second) mask layer of silicon dioxide using CVD because Kim teaches that this is a conventional deposition method for this material". As applicants described in their specification, and as claimed in Claims 9, 18, and 25, CVD SiO_2 is only one of many masking materials which may be used. Other materials include TEOS, Si_3N_4, BSG, PSG, BPSG, and mixtures thereof. Applicants recited the use of CVD SiO_2 in Claim 6, because this method of producing a mask integrates nicely with other deposition processes used to form the starting structure used by applicants, of the kind shown in Figures 1 and 2.

Applicants' claimed method is clearly distinguishable from the method described and claimed in the Ye et al. reference, and is clearly distinguishable from the method described and claimed in the Kim et al. reference. A combination of these references will not motivate one skilled in the art to make applicants' invention.

The above combination of references is another example of an instance where individual teachings are taken from unrelated references to try to render obvious applicants' invention. One skilled in the art of RAM capacitors is unlikely to combine these references, but even if the references are combined, it is well established in case law that "obvious to try" does not meet the requirement under 35 U.S.C. § 103 for obviousness. "The mere need for experimentation to determine parameters needed to make a device work is an application of the often rejected obvious-to-try standard and falls short of the statutory obviousness of 35 U.S.C. §103." (*Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988).) "An 'obvious-to-try' situation exists when a general disclosure may pique the scientist's curiosity, such that further investigation might be done as a result of the disclosure, but the disclosure itself does not contain a sufficient teaching of how to obtain the desired result or indicate that the claimed result would be obtained if certain directions were pursued." (*In re Eli Lilly & Co.*, 902 F.2d 943, 14 U.S.P.Q. 2d 1741 (Fed.Cir. 1990).) In the present instance, the combination of references cited does not even suggest to one skilled in the art which process variables or materials should be selected to arrive at applicants' invention. It is only with the hindsight of applicants' disclosure that the Examiner has gone to disparate subject matter and selected individual process steps which might be useful in applicant's method.

In light of the above distinctions and arguments, applicants respectfully request withdrawal of the rejection of Claims 6, 9, 18, and 25 under 35 USC § 103(a) over Ye et al., and further in view of Kim et al.

Claims 7 and 8 are rejected under 35 USC § 103(a) as being unpatentable over Ye et al., in view of Hong et al., as applied to Claims 2 or 4, and further in view of Kim et al.

Applicants respectfully contend that Claims 7 and 8 which pertain to the composition of the mask layer and the substrate and to the composition of the mask layer, respectively, are not obvious in view of the combination of the Ye et al., Hong et al., and Kim et al. references. The distinctions

between the Ye et al. and Kim et al. references which were made above with respect to Claims 6, 9, 18, and 25 apply with respect to Claims 7 and 8. In addition, the Hong et al. reference which pertains to a combination of wet and dry etch steps (while applicants' invention does not employ wet etch steps) has been distinguished above. A combination of these three references does not make applicants' invention as claimed in Claims 7 and 8 obvious.

In detail, Claim 7 recites the method of Claim 2 wherein the mask layer and substrate layer each comprise CVD SiO_2. Claim 8 recites the method of Claim 4, wherein the mask layer comprises CVD SiO_2. Both Claims 2 and 4 depend from Claim 1. The deficiencies of the disclosures of Ye et al., Hong et al., and Kim et al. with respect to the patentability of the present invention are discussed above with respect to the recitation of the elements of Claim 1. The combination of the recitations of Claims 1, 2 and 7, or the combination of the recitations of Claims 1, 4, and 8 is not obvious over the combination of Ye et al., Hong et al., and Kim et al. when this combination of references does not render Claim 1 obvious.

In light of the above distinctions, applicants respectfully request withdrawal of the rejection of Claims 7 and 8 under 35 USC § 103(a), over Ye et al., in view of Hong et al., and further in view of Kim et al.

Claim 21 is rejected under 35 USC § 103(a) as being unpatentable over Ye et al., in view of Anderson, Jr. et al. and Kornblit et al., as applied to Claim 19, and further in view of Kim et al.

Applicants respectfully submit that Claim 21 is not obvious over this combination of references. Claim 21 recites the various materials which may be used to form the mask layer recited in independent Claim 19. The distinctions between the invention claimed in Claim 19 and the disclosures of Ye et al., Anderson, Jr. et al., and Kornblit et al. were discussed in detail with reference to Claim 19 above. As previously mentioned, the Kim et al. reference merely mentions that CVD is one of the techniques used to deposit silicon oxide. The addition of a recitation of the materials which may be used to form the mask layer in applicants' invention, many of which do not

include silicon oxide, combined with the recitation of the series of process steps in Claim 19 does not render Claim 21 obvious. Since the teachings of Ye et al., Anderson, Jr. et al., and Kornblit et al. do not render the integrated process steps of Claim 19 obvious, and the teachings of Kim et al. add nothing to these teachings which would direct one skilled in the art to the integrated process Claimed in Claim 19, this combination of references does not make Claim 19 obvious. Adding a recitation of a listing of materials from which the inorganic mask may be formed to the steps recited in Claim 19 does not render Claim 21 obvious when Claim 19 is not obvious.

In light of the above distinctions, applicants respectfully request withdrawal of the rejection of Claim 21 under 35 USC § 103(a) over Ye et al., in view of Anderson, Jr. et al. and Kornblit et al., and further in view of Kim et al.

Claim 20 is rejected under 35 USC § 103(a) as being unpatentable over Ye et al., in view of Anderson, Jr. et al. and Kornblit et al., as applied to Claim 19, and further in view of U.S. Patent No. 5,613,296, to Kurino et al.

Claim 20 recites the method of Claim 19 wherein the method additionally comprises a step of etching the etch stop layer underlying the barrier layer. As previously discussed in detail, the Ye et al., Anderson, Jr. et al., and Kornblit et al. reference combination does not render Claim 19 obvious. The addition of the Kurino et al. reference, which pertains to a dual damascene process for forming multilayered interconnects does not render Claim 20 obvious. The Kurino et al. reference teaches a method for the concurrent formation of contact and via holes in a single sequence of operations. This reference teaches another process which is totally unrelated to the formation of RAM capacitors and recites a series of steps which are not related to applicants' invention. The addition of this reference to the Ye et al., Anderson Jr. et al., and Kornblit et al. references does not lead one skilled in the art to applicants' invention.

In detail, the Kurino et al. reference describes a method for concurrent formation of contact and via holes. In order to facilitate the fabrication of wiring layers in integrated circuit devices, the

conductive path interconnections between areas of conduction on three layers (the three layers being separated by insulating layers) of the integrated circuit are fabricated during the same sequence of operations. The regions of conduction can be associated with the surface of a semiconductor substrate along with associated components fabricated thereon and two wiring layers, or the regions of conduction can be associated with three wiring layers. After the second insulating layer is formed, but before the formation of the final conductive layer, holes are created, a portion of the holes extending through the second insulating region to the prior wiring layer, and a portion of the holes extending through the second insulating layer and through the first insulating layer to a semiconductor substrate or to an initial wiring layer. In order to provide a conductive plug for high aspect holes, a final conductive layer is formed, and pressure is applied to the final conductive layer, forcing the conductive material into the holes. The conductive material remaining is patterned and etched to form a final wiring layer. (Abstract)

Kurino et al. is cited by the Examiner as teaching that forming conductive paths through two insulating layers at the same time permits a reduction in the number of patterning and etching steps. The Examiner states "It would have been obvious to one of ordinary skill in the art to etch the substrate, in the method of Ye in view of Anderson and Kornblit (including the silicon dioxide etch stop overlying the silicon wafer) or in the method of Ye, at the same time as etching the barrier layer because Kurino teaches that this will reduce the number of patterning and etching steps".

As discussed above, applicants' claimed method is clearly distinct from the method disclosed by Ye et al., and is not obvious over the method disclosed by Ye et al. Further, the addition of the disclosures of Anderson, Jr. et al., and Kornblit et al. do not lead to applicants' invention. The Kurino et al. method pertains to another process which is totally unrelated to the formation of RAM capacitors of the kind described in applicants' invention. A combination of the teachings of each cited reference as a whole is more confusing than helpful, since the methods in the various references involve different process steps used in a different order than applicants' method, to produce a

different result. One skilled in the art would not look at these references and conclude that a method of forming a RAM capacitor is obvious.

The Examiner is respectfully requested to forget what she has learned from applicants' disclosure; to simply look at the four references being cited together; and, to see whether she believes the combination of these references teaches an integrated series of method steps useful in forming a RAM capacitor. It is not permitted to use applicants' disclosure as a blueprint from which to search the art for recited individual steps in the art and then to combine these steps into an integrated process taught by applicants, when none of the individual references even indicates that the step selected by the Examiner from that reference might be placed into an integrated process of the kind taught by applicants.

In light of the above distinctions, applicants respectfully request withdrawal of the rejection of Claim 20 under 35 USC § 103(a), over Ye et al., in view of Anderson, Jr. et al. and Kornblit et al., and further in view of Kurino et al..

Claim 28 is rejected under 35 USC § 103(a) as being unpatentable over Ye et al., as applied to Claim 22, and further in view of Kurino et al.

Claim 28 depends from Claim 22, and merely indicates that the substrate underlying the barrier layer may be etched during etching of the barrier layer. The deficiencies of the disclosures of Ye et al. and Kurino et al. with respect to the patentability of the present invention are discussed above. Claim 28 is not obvious over the combination of Ye et al. and Kurino et al. for the same reasons that Claim 22 is not obvious over Ye et al.

In light of the above distinctions, applicants respectfully request withdrawal of the rejection of Claim 28 under 35 USC § 103(a), over Ye et al., and further in view of Kurino et al.

Claim 24 is rejected under 35 USC § 103(a) as being unpatentable over Ye et al., as applied to Claim 22, and further in view of U.S. Patent No. 4,544,602, to Kobayashi et al.

Claim 24 depends from Claim 22 and recites the various materials which are preferred for formation of the first mask layer. The distinction between the Ye et al. reference which requires the use of an organic material between a inorganic masking layer an underlying substrate and applicants' invention where the inorganic masking layer is applied directly over the substrate has been discussed above. One skilled in the art reading the teachings of Kobayashi et al. will immediately see that the device being fabricated is a magneto-optical recording medium. (Abstract) Figure 1 shows a schematic of a typical starting substrate which includes a transparent substrate 1, a magnetic film layer 2, and a reflection film layer 3 formed on the magnetic film layer 2. The overall composition for these starting materials is presented at Col. 3, lines 4 - 26, which illustrates how different the combination of materials used by Kobayashi et al. is from the combination of materials being used by applicants. One skilled in the art would not even select this reference when considering materials and processes to be used to fabricate RAM capacitors of the kind described by applicants. Combining the Ye et al. reference with the Kobayashi et al. reference does not render applicants' series of integrated method steps obvious.

In detail, the Kobayashi et al. reference pertains to a magneto-optical recording medium which comprises a transparent substrate, a vertical magnetic-anisotropic magnetic film layer formed on the transparent substrate, and a reflection layer formed on the vertical magnetic-anisotropic film layer. (Abstract) The Examiner cites Kobayashi et al. as teaching that silicon nitride and tantalum nitride may both be used as the material for a protective layer overlying a metal layer. However, when the overall starting structure is different, the fabrication processes involved are different, and the resulting product is different, there is no reason for one skilled in the art to select a particular material from an unrelated reference for substitution into applicants' method.

In light of the above distinctions, applicants respectfully request withdrawal of the rejection of Claim 24 under 35 USC § 103(a), over Ye et al., and further in view of Kobayashi et al.

Applicants believe that the presently pending claims as amended are in condition for allowance, and the Examiner is respectfully requested to enter the requested amendments and to pass the application to allowance.

The Examiner is invited to contact applicants' attorney with any questions or suggestions, at the telephone number provided below.

Respectfully submitted,

Shirley L. Church

Shirley L. Church
Registration No. 31,858
Attorney for Applicants
(650) 473-9700

Correspondence Address:
Patent Counsel
Applied Materials, Inc.
P.O. Box 450-A
Santa Clara, CA 95052